ABSTRACT OF THE DISCLOSURE

A semiconductor integrated circuit is disclosed, in which a plurality of circuit blocks each having a clock distribution line pattern, a first signal path for transmitting the data signal from a first circuit block to a second circuit block, a second signal path for transmitting a clock signal, at least a first buffer circuit connected to the first signal path to constitute the first signal path, and a second buffer circuit connected to the second signal path to configure the second signal path are formed on a single semiconductor chip. The first and second signal paths have the same length, and data and clock are transmitted in parallel to each other on the first and second signal paths, respectively. The second circuit block latches the received data by the clock transmitted in parallel.